A 50% Lower Power ARM Cortex CPU using DDC Technology with Body Bias

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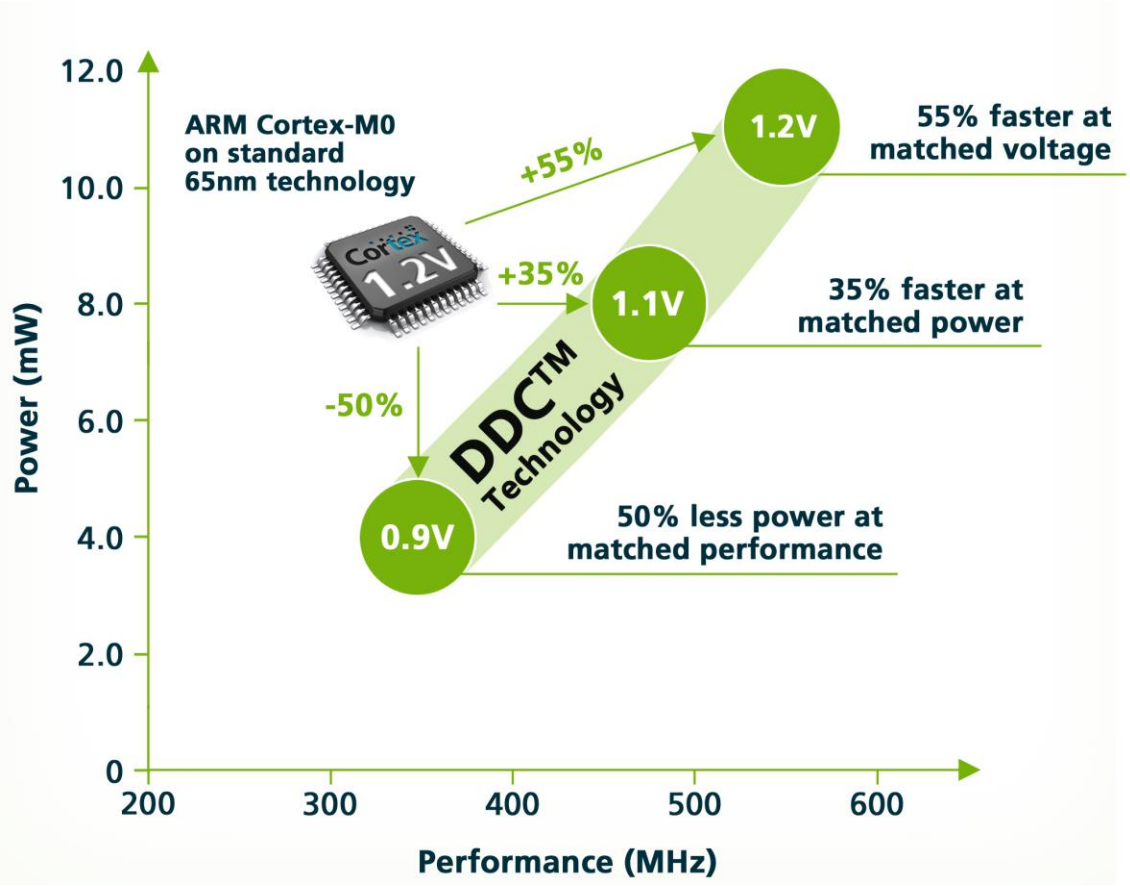
August 26, 2013

Agenda

- DDC transistor and PowerShrink platform overview
- ARM Cortex-M0 implementation and results
- Application of DDC technology to HKMG nodes



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Deeply Depleted Channel™ (DDC) Transistor

1

Undoped/lightly doped region

- Improved matching (low RDF)
- Higher mobility (↑ $I_{D,lin}$)
- Higher analog gain (↑ g_m)

2

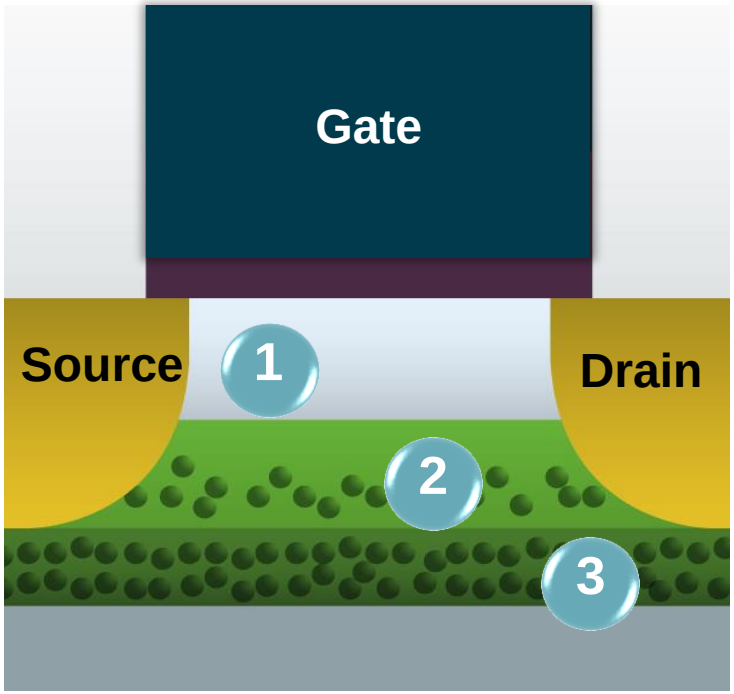
V_T setting offset region

- Multiple V_T on chip

3

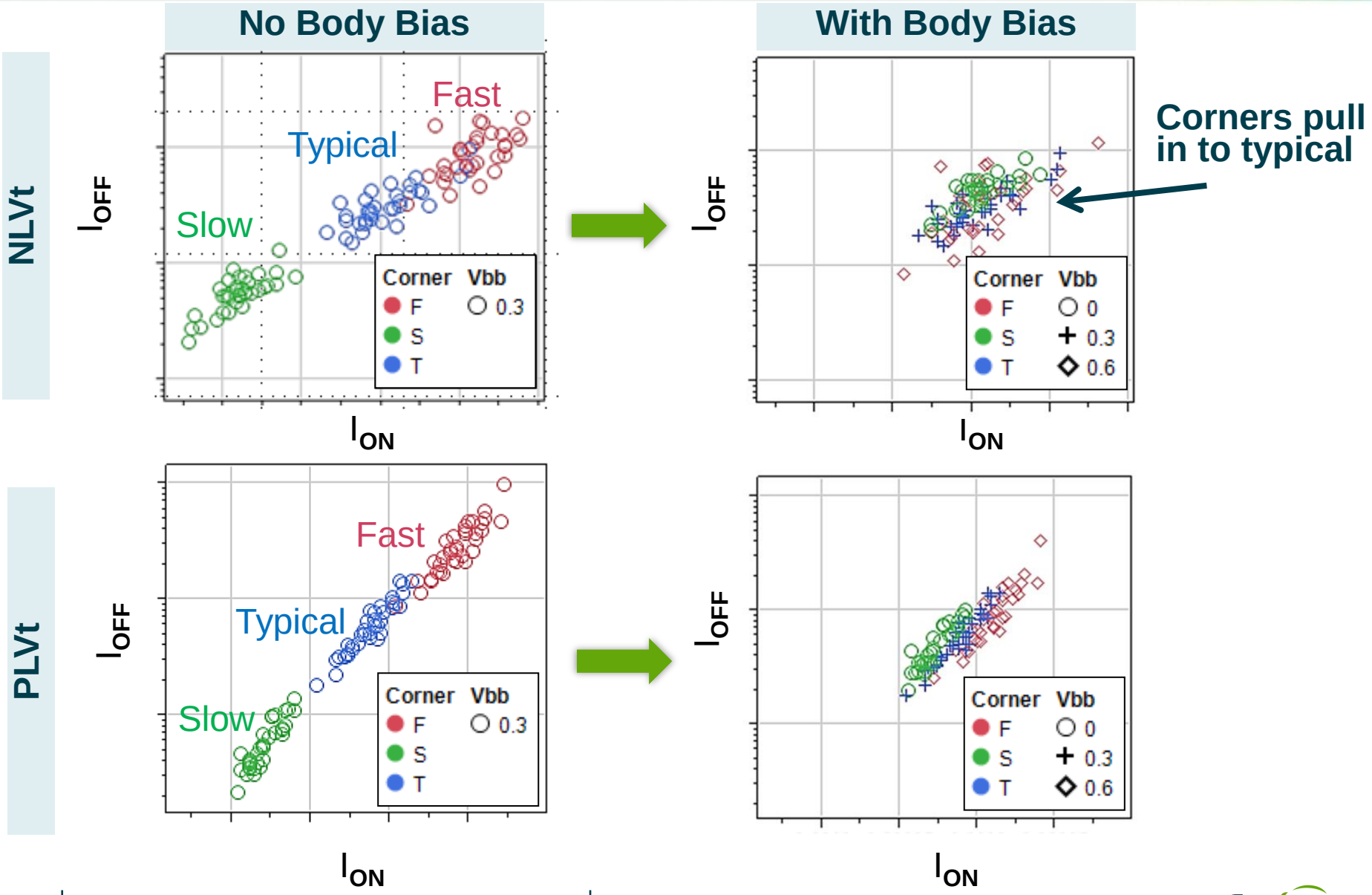
Screening region

- Superior scalability
- Improved drive current (↑ I_{eff} ↓ DIBL)
- Higher analog gain (↑ R_{out})
- Strong body coefficient (corner pull-in)

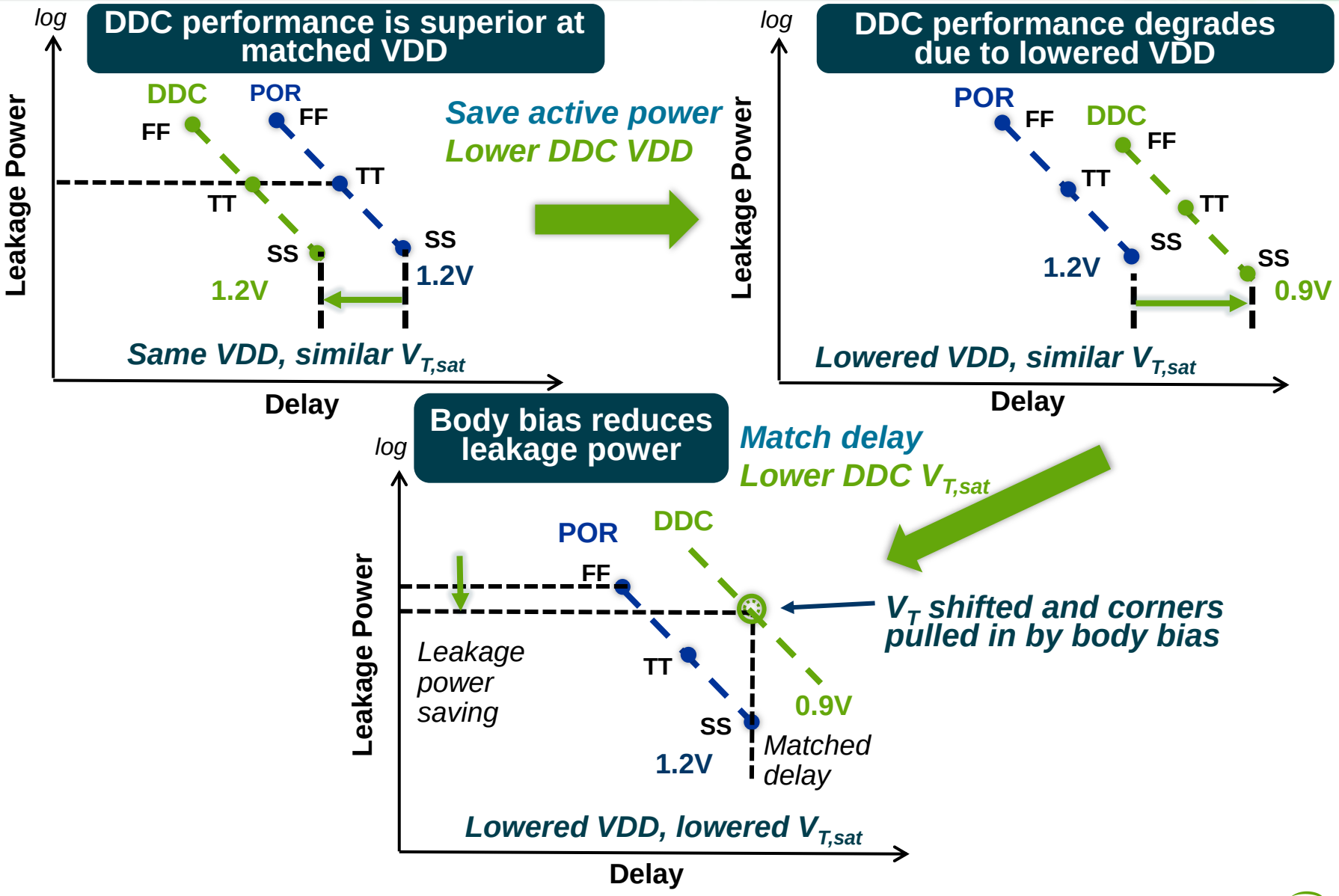


One example, not drawn to scale

Corner Pull-in with Body Bias



DDC PowerShrink Platform: Save Active and Leakage Power Using Body Bias



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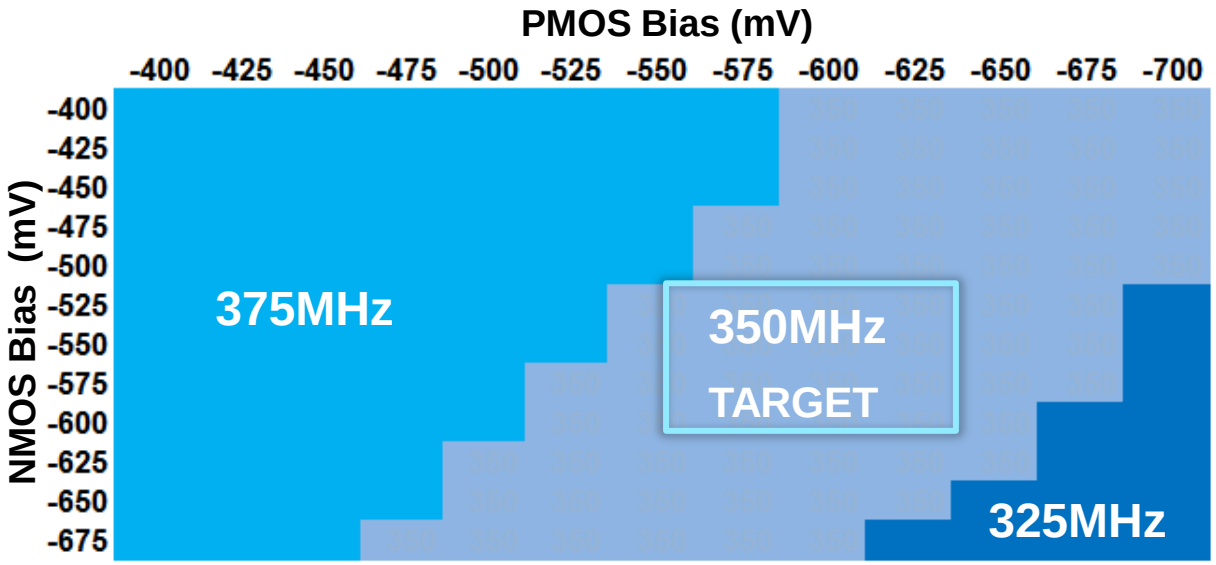
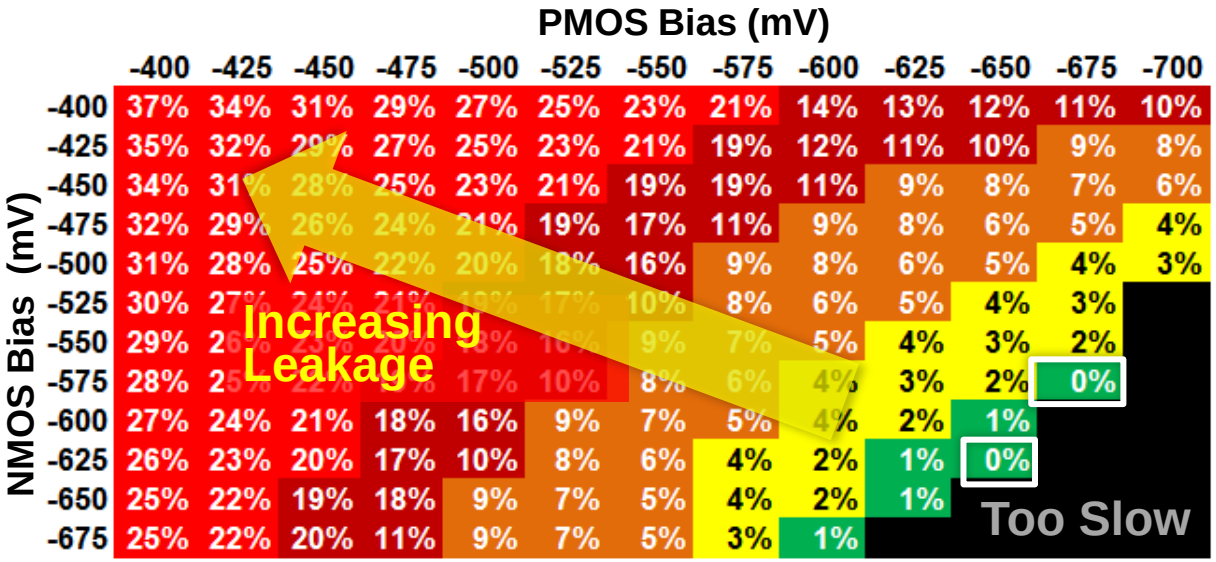
ARM Cortex-M0 CPU Bias Targeting



Measured ARM Cortex-M0
Speed and power response to bias

Speed



- Target 350MHz
- Many bias voltages achieve the target frequency but power is not optimal at all biases

Leakage (delta to optimal)

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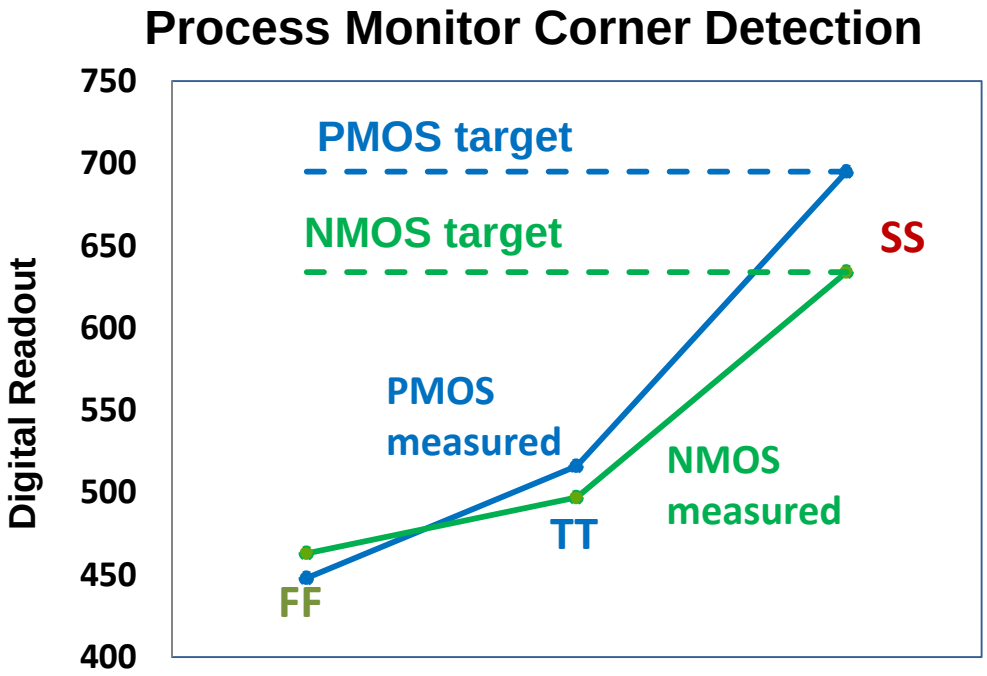
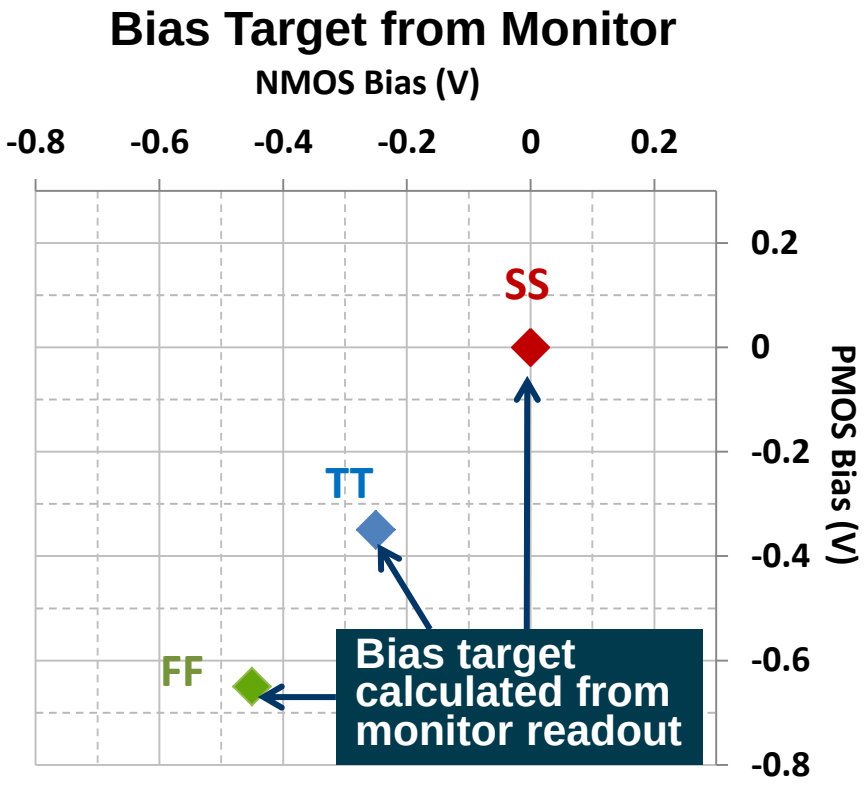
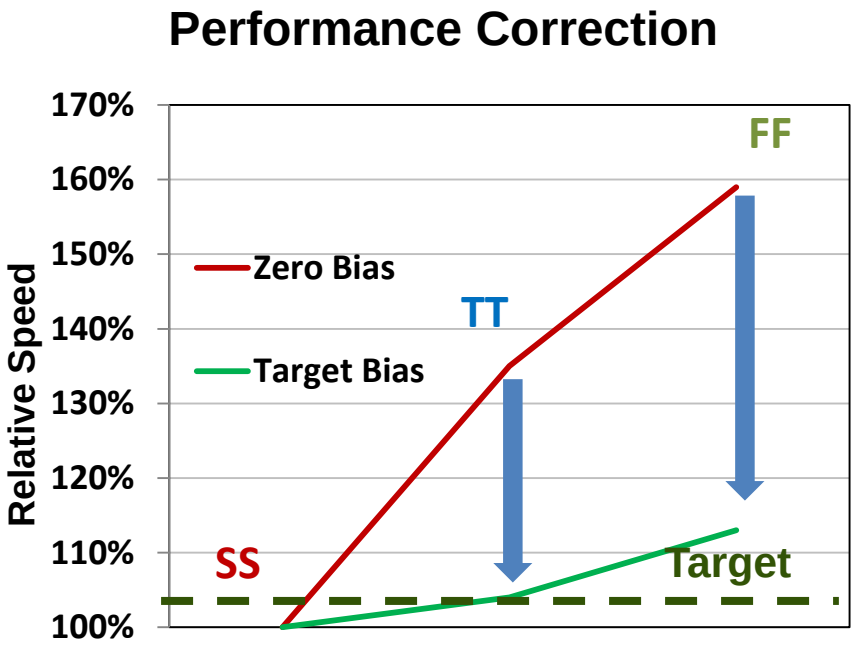
Process Monitor Bias Targeting (55nm Measured)

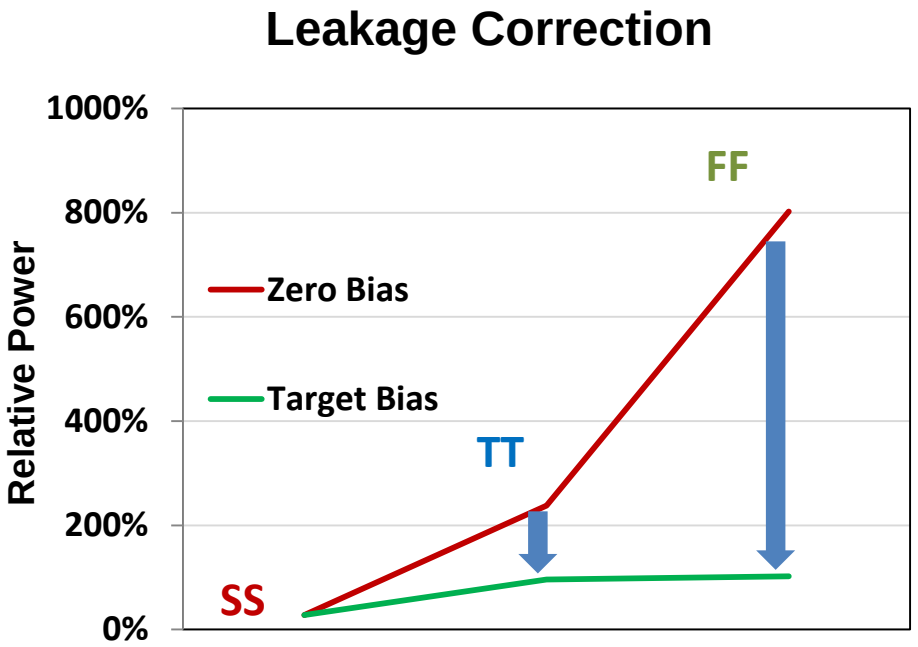


- Process Monitor independently measures NMOS and PMOS corners
- Digital readout correlates to corner
- Bias voltage is calculated from readout



Process Monitor Bias Targeting (55nm Measured)

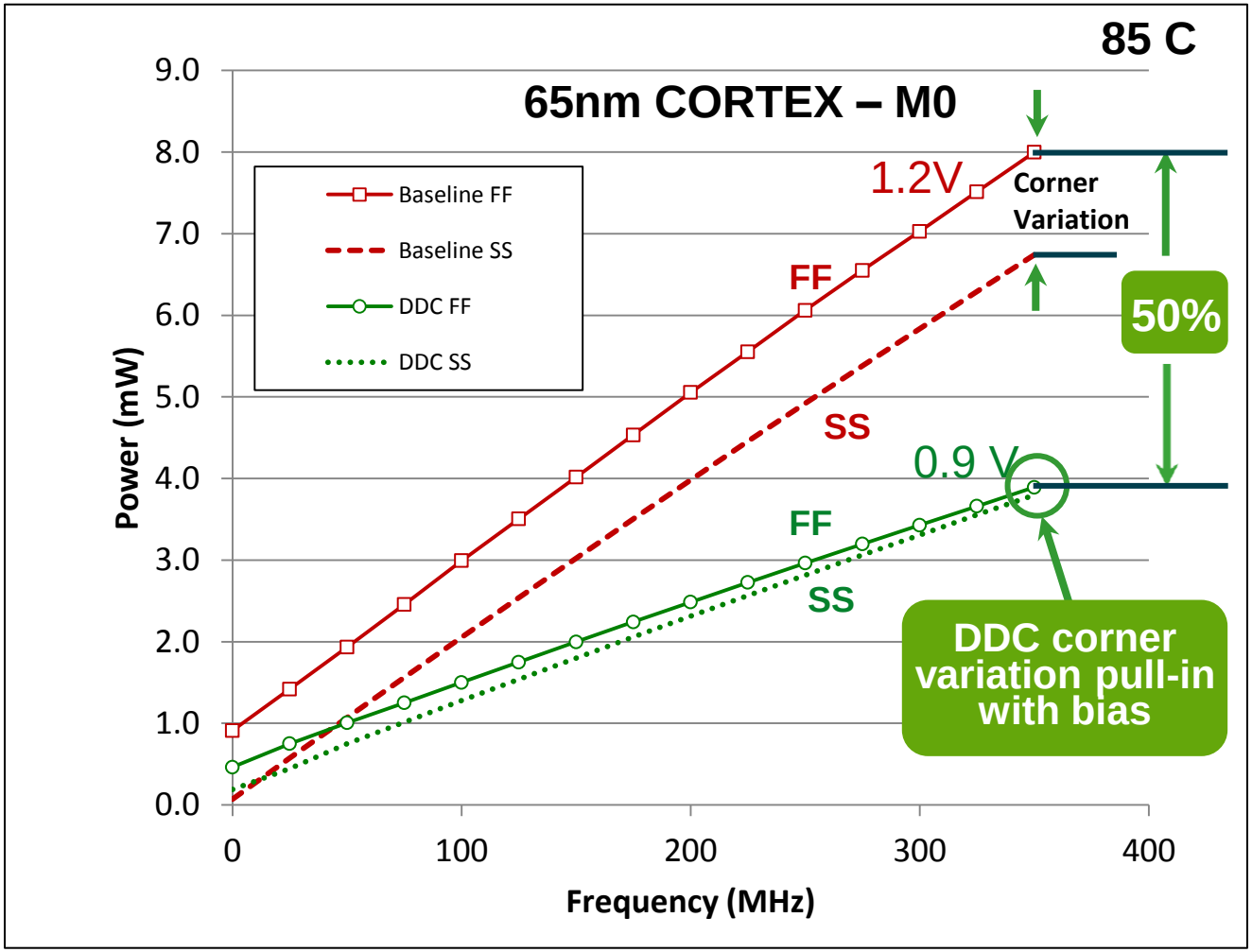




- Performance is corrected to 13% faster than target
- Fast corner leakage is corrected to the same point as typical

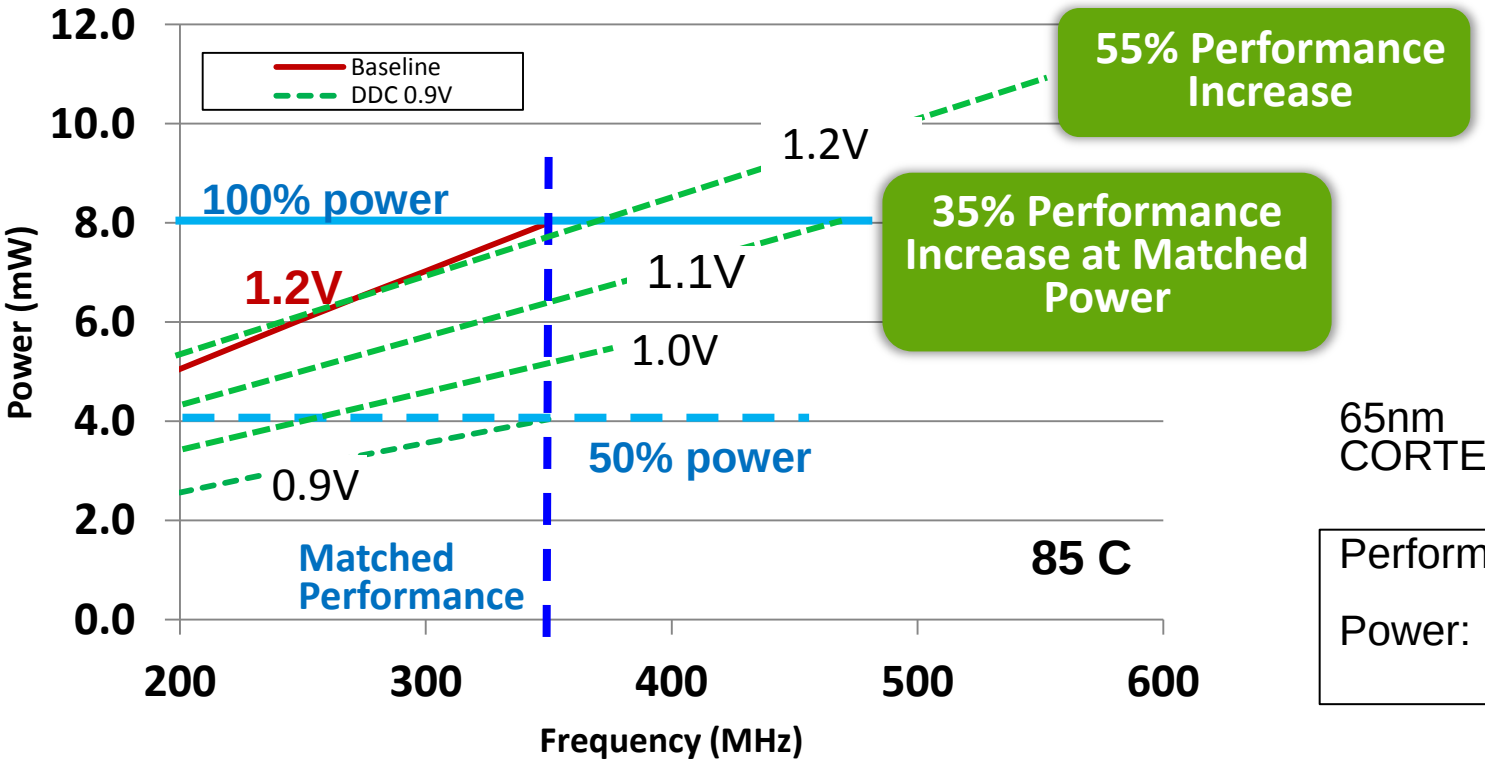
PowerShrink Platform: ARM Cortex-M0 CPU

- 50% power vs baseline at FF (leakage and dynamic)
- Matched performance at SS



Tunable Power / Performance

- Matched performance at 50% power **0.9V**
- +35% performance at matched power **1.1V**
- +55% performance at matched voltage **1.2V**



65nm
CORTEX – M0

Performance:
SS corner
Power:
FF corner

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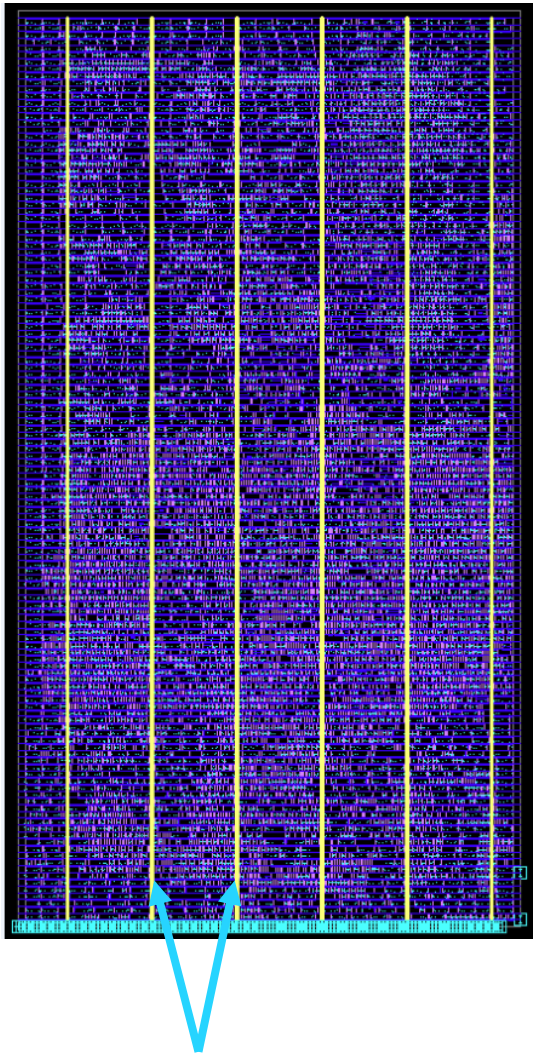
ARM Cortex-M0 Body Bias Network Implementation



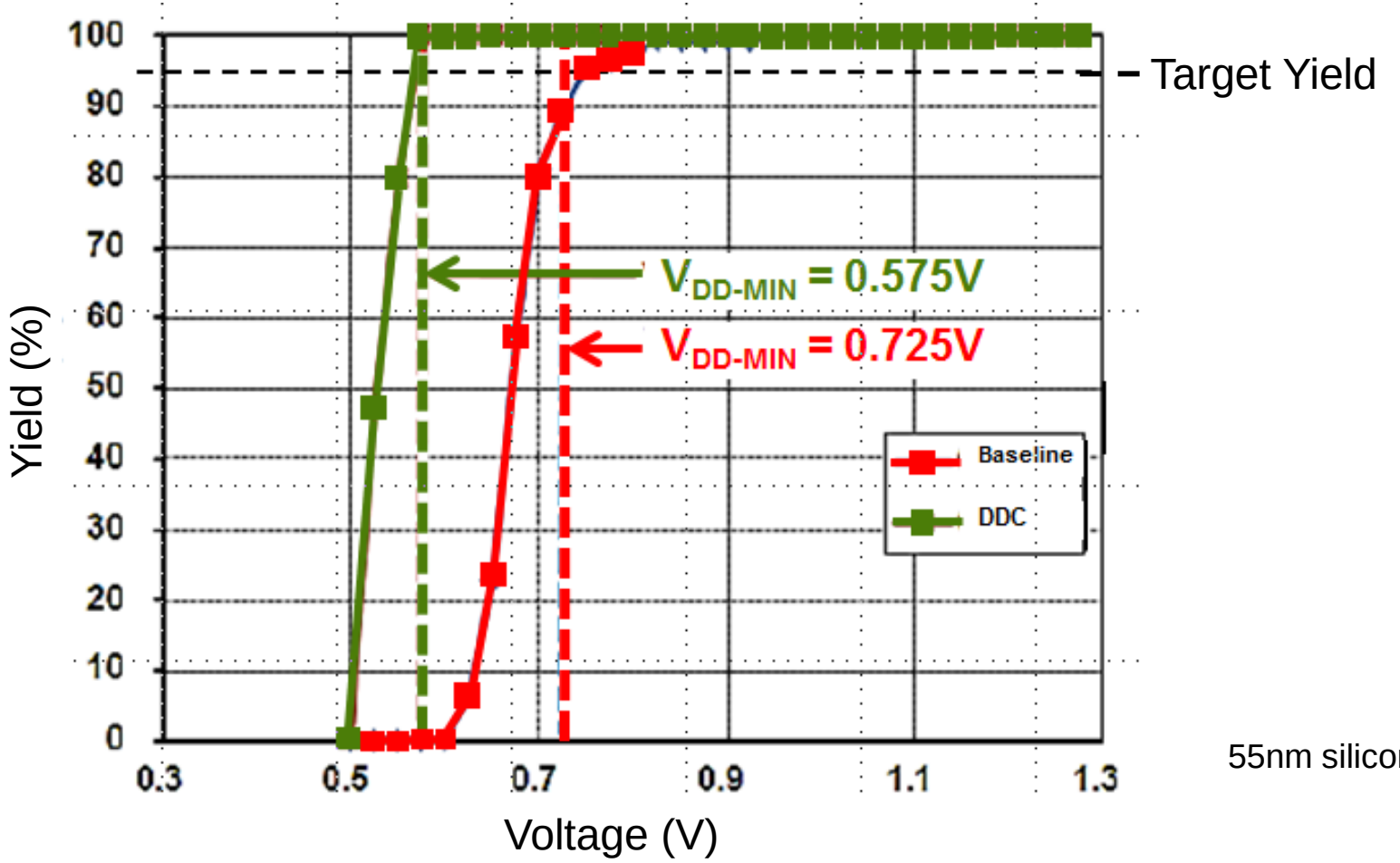
- Minimal routing resources used for bias network
  - Route in columns
  - Double-space bias wires for reliability
  - 1 PMOS wire, 1 NMOS wire

Vertical Track Usage per Column

Layer	Available Tracks	Bias Tracks
M2	300	4
M4	300	0
Total	600	4 (0.7%)

Lower SRAM $V_{DD\text{-}min}$ Enables Low-V_{DD} Operation

- $V_{DD\text{-}min}$ of 8Mb SRAM lowered by 150mV at 125°C
- Production 55nm SRAM data



55nm silicon

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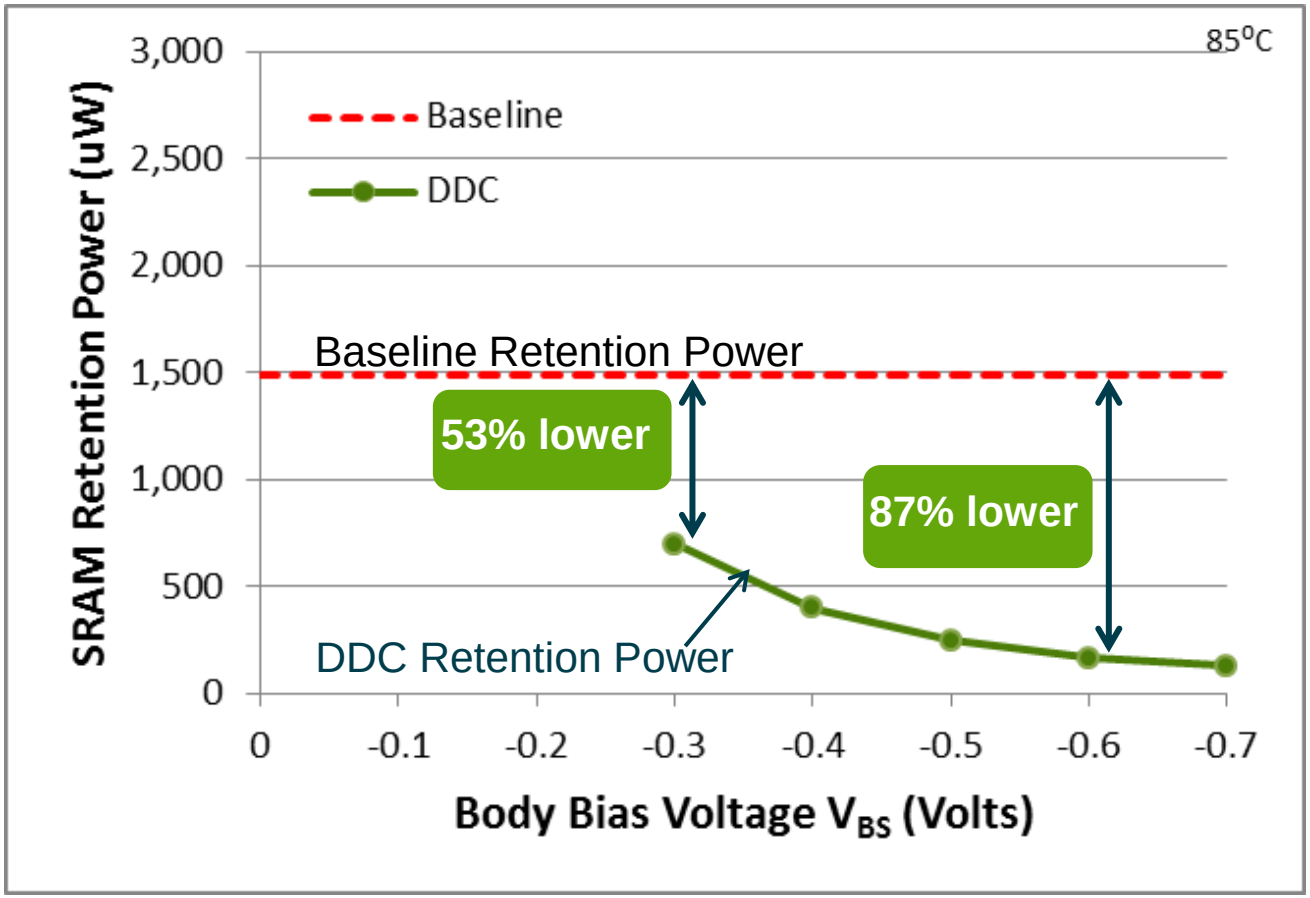
Lower SRAM Retention Power

- 50% less leakage in Standby and Retention modes at nominal V_{BS}
- More than 5X less leakage in Retention mode with V_{BS} = -0.6V



65nm silicon

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DDC Technology in Silicon Gate and HKMG

Silicon-Gate

DDC™ PowerShrink™
Memory

DRAM	**Other**

DDC™ PowerShrink™
90nm, 65nm, 55nm, 40nm

Imaging	CPU	
WiFi	RF	
Mixed Signal	Display Drivers	GPS

SuVolta®
Deeply Depleted Channel™ (DDC) Technology

Metal-Gate

DDC™ PowerShrink™
28nm, 20nm

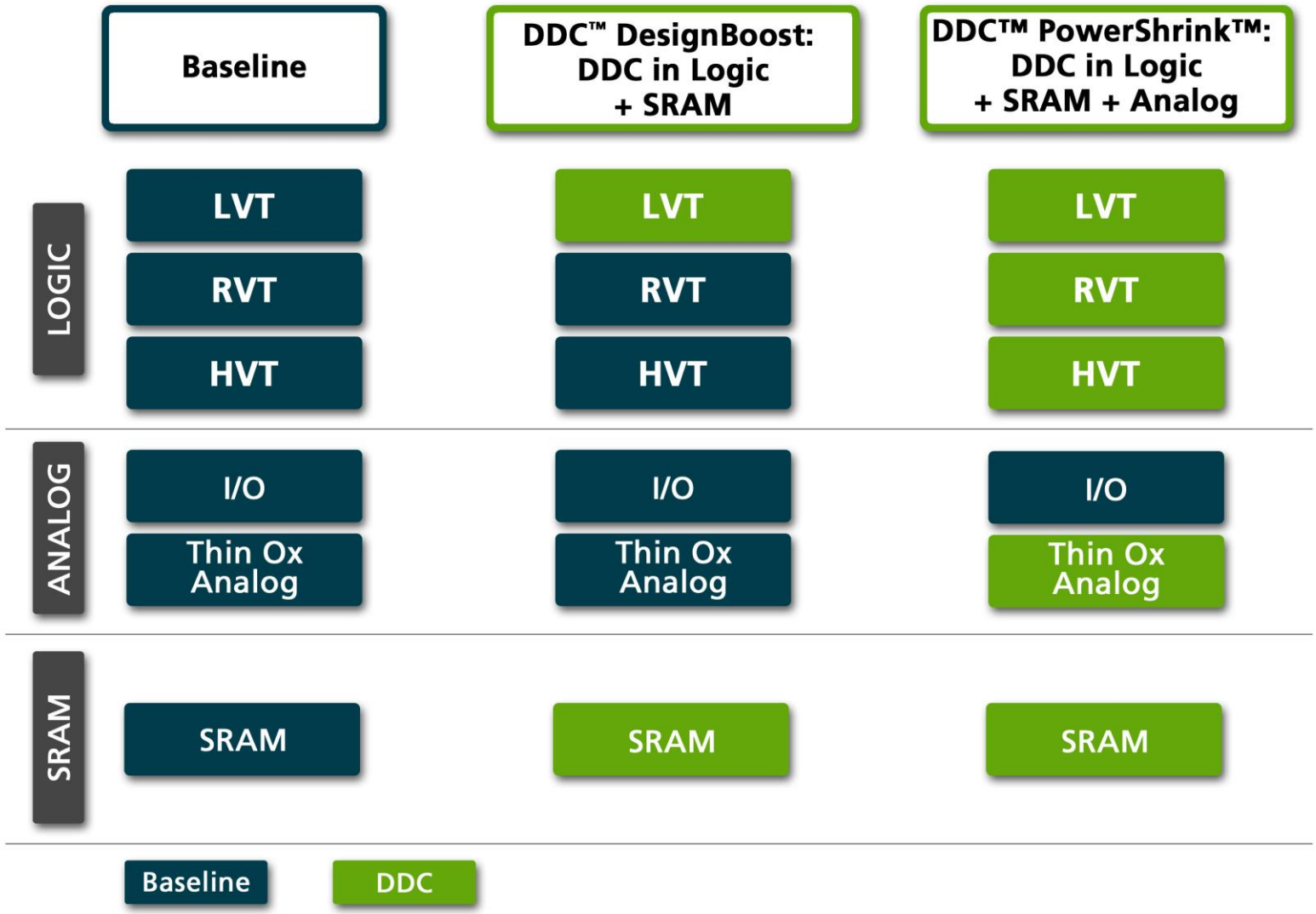
CPUs + GPUs	Networking
SoC	FPGA

DDC™ DesignBoost
28nm, 20nm

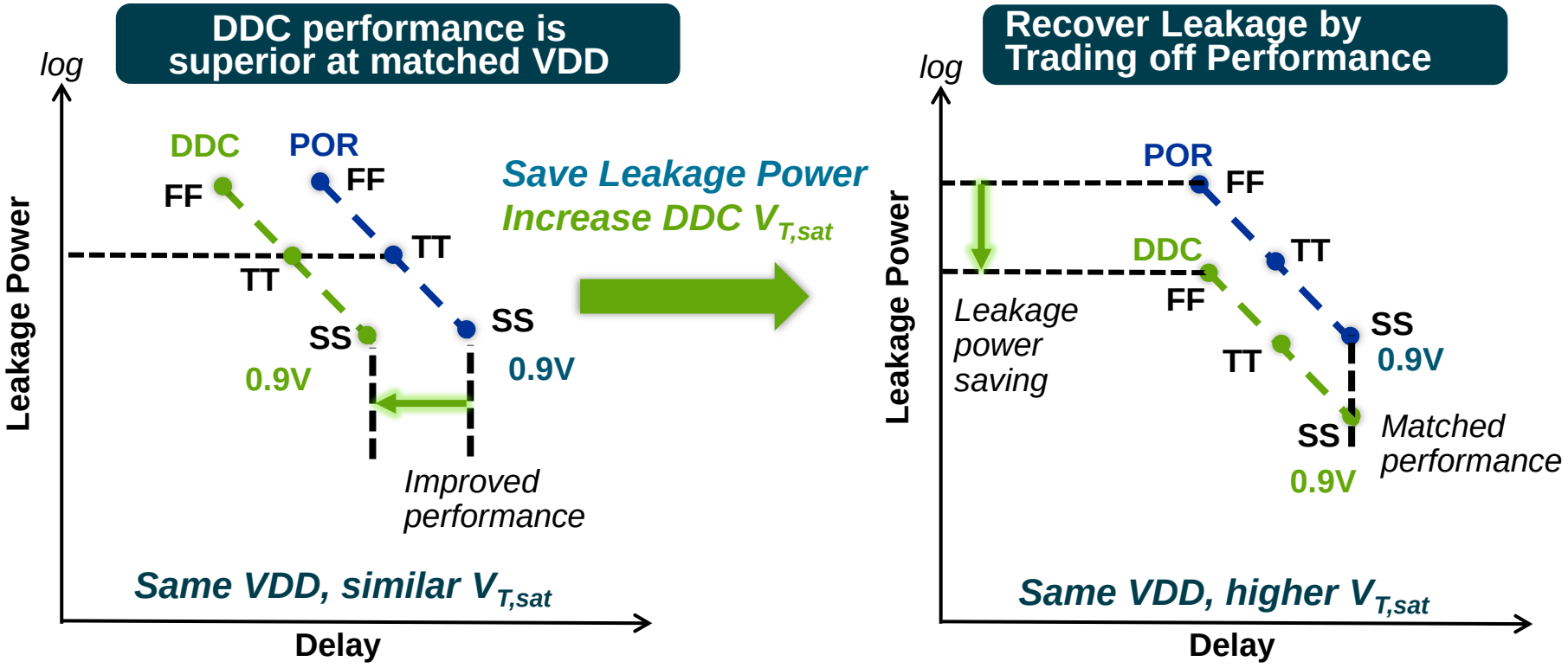
CPUs + GPUs	Networking
SoC	FPGA

Proven, Legacy — **Technology Nodes** — **Advanced**

DDC Technology Modular Implementation



DDC DesignBoost: Target Leakage Power Savings



DDC DesignBoost

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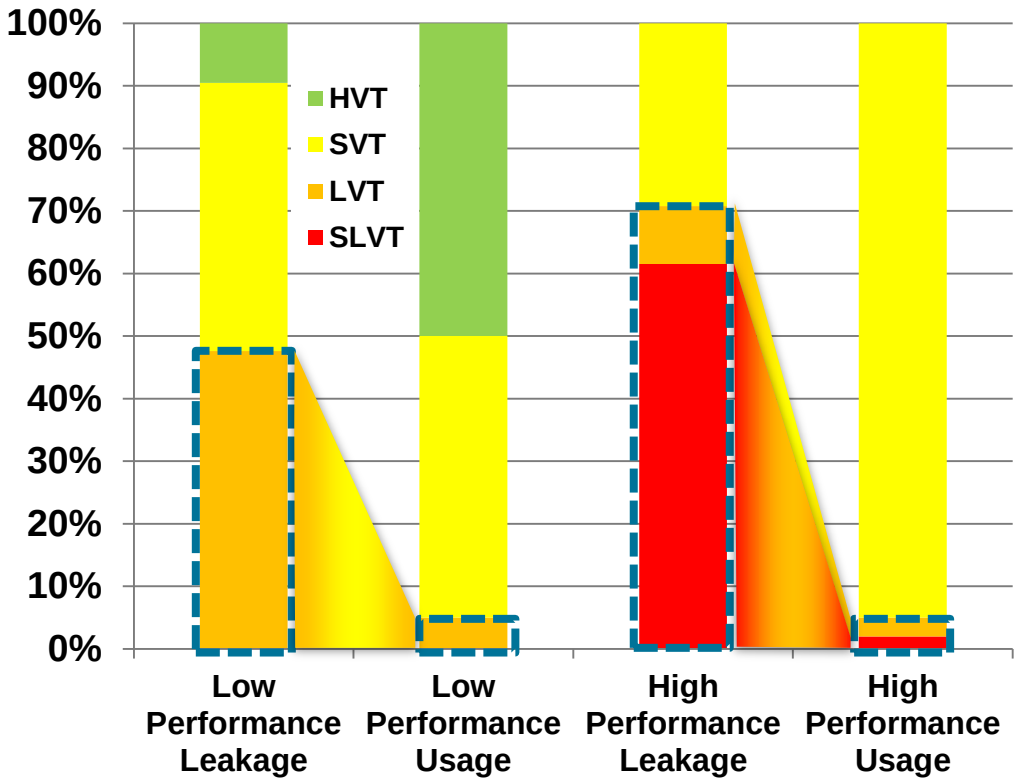
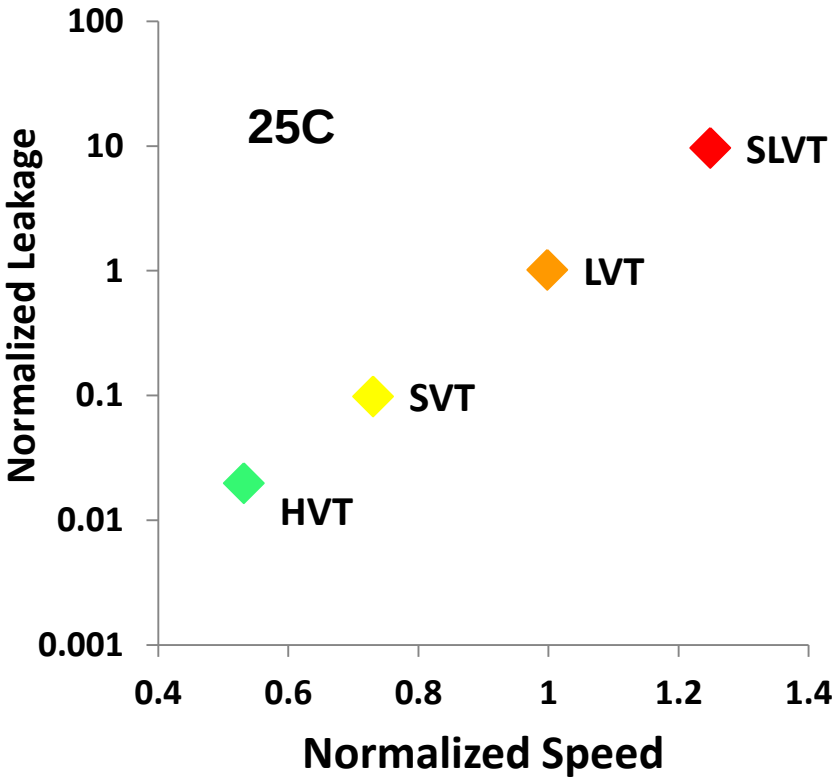
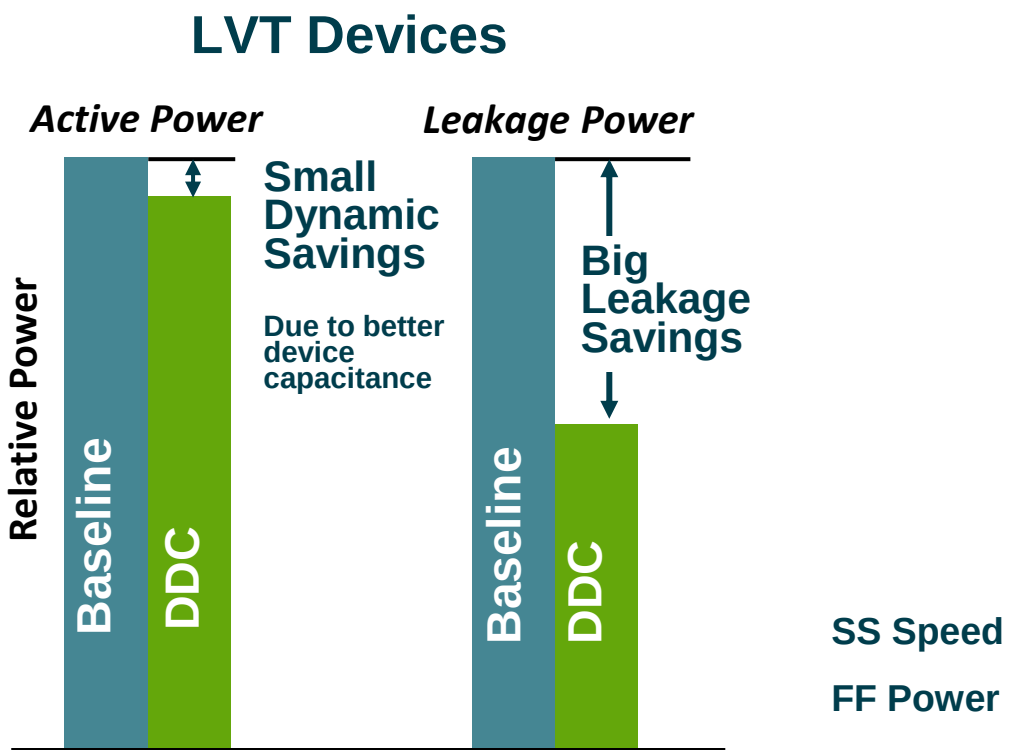
DDC DesignBoost Motivation





- LVT and SLVT devices contribute a large portion of the leakage power at advanced nodes
- Leakage power reduction is a key value adder for high performance designs

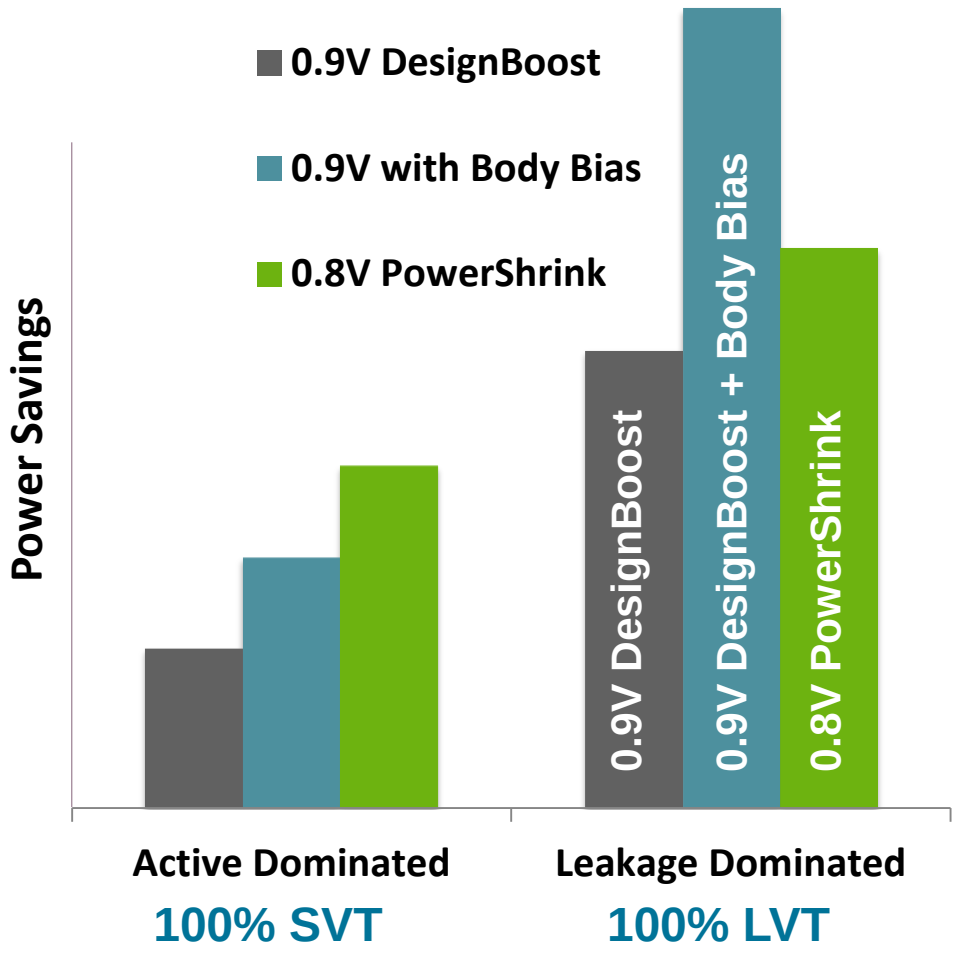
DDC DesignBoost Power Savings in HKMG



DDC DesignBoost

Target matched performance to reduce Ioff

HKMG Power Analysis



- HKMG design
  - 10% activity factor
- DDC DesignBoost
  - No design change
  - Body Bias improves power savings
- PowerShrink platfrom
  - For active power dominated circuits

125C

SS Speed

FF Power

All transistors are DDC transistors

Summary

- ARM Cortex-M0 validated at 65nm
  - Matched performance at 50% power
  - +35% performance at matched power
  - +55% performance at matched voltage
- SRAM validated at 65nm and 55nm
  - 150mV Vmin reduction in production 55nm SRAM
  - Less than 50% static power in standby and retention
- DDC technology demonstrated at advanced HKMG nodes
  - Lower static power at matched performance
  - Lower active power with body bias